REMARKS

In response to the Office Action mailed on 02/06/06, Applicant wishes to enter the following remarks for the Examiner's consideration. Applicant has amended claims 1, 5 and 6. Claims 1-13 are pending in the application.

Rejection of claims under 35 USC §112

Claim 1 has been rejected under 35 USC §112, second paragraph, as being incomplete. Claim 1 has been amended to clarify that the identifiers and the modified sequence are stored in a computer readable medium. In light of the amendment, Applicant respectfully submits that the 35 USC §112, second paragraph, rejection of claim 1 has been overcome and requests that this basis of rejection of the claims be withdrawn and that a Notice of Allowance for these claims be mailed at the Examiner's earliest convenience.

Claims 1, 6 have been rejected under 35 USC §112, second paragraph, as being incomplete for failing to include storing the multiple instruction control words. Applicant respectfully traverses this rejection of the claims. The method of claim 1 may be performed manually or automatically. If the method of claim 1 is performed by a person, rather than a computer, a separate recitation of storing the multiple instructions words is not essential. The instructions could be written on a piece of paper or held in the head of the person performing the compression, for example. In light of these remarks, Applicant respectfully submits that the 35 USC §112, second paragraph, rejection of claim 1 has been overcome and requests that this basis of

rejection of the claims be withdrawn and that a Notice of Allowance for these claims be mailed at the Examiner's earliest convenience.

Rejection of claims under 35 USC §101

Claims 1, 6 have been rejected under 35 USC §101 as being directed towards non-statutory subject matter. Applicant respectfully traverses this rejection of the claims in view of the amendments to claims 1 and 6.

Claim 1, as amended, is directed towards the production of a computer readable medium containing a compressed sequence of multiple-instruction control words. Applicant submits that the computer readable medium is a useful, concrete and tangible result of the process of claim 1.

Claim 6 has been amended to include the element of the processor executing the decompressed control word. Thus, execution is achieved yielding a useful, tangible result.

In view of the amends to claims 1 and 6, applicant respectfully submits that the 35 USC §101 rejection of claims 1 and 6 have been overcome and requests that this basis of rejection of the claims be withdrawn and that a Notice of Allowance for these claims be mailed at the Examiner's earliest convenience.

Rejection of claims under 35 USC §102

Claims 1, 4-6 and 8-12 have been rejected under 35 USC §102(b) as being anticipated by Tanaka (Patent No. US 5,893,143). Applicant respectfully traverses this rejection of the claims.

Claims 1, 4 and 5. Referring to Figure 1 of the specification, an aligned field is a field that is in the same position in every control word of the sequence. For example, the field 4 in Figure 1 is an aligned field. The first element of the claim 1 calls for identifying a set of *aligned* fields that contain NOP instructions in *each* control word of the *sequence* of multiple-instruction control words. Thus, field 4 contains a NOP instruction in *each* of the 4 instruction words (VLIW 1, VLIW 2, VLIW 3 and VLIW 4). The sequence of multiple-instruction control words is therefore modified to remove the set of aligned fields denoted as field 4, as shown in Figure 2. In contrast, aligned field 2 contains NOP instructions, but not in each of the instruction words (VLIW 1 is not an NOP instruction). Therefore, field 2 is not removed (as indicated in Figure 2). The compressed sequence contains the same number of words as the original sequence, but has fewer fields.

In contrast, the Tanaka reference examines single instruction words to identify and remove NOP codes. None of the field (a, b, c and d) in the element 700 of figure 6 of Tanaka contain NOPs in each of the words 0-4, so Tanaka does not teach the element of identifying a set of aligned fields that contain NOP instructions in each control word of the sequence of multiple-instruction control words. Further Tanaka does not teach the element of modifying the sequence of multiple-instruction control words to remove the set of aligned fields. The element 701 in Figure 6 of the Tanaka reference shows that the number of instruction words has been reduced from 5 to 3 while the number of fields remains at 4. Thus, no aligned fields have been removed.

Claim 4 depends from claim 1. Although additional arguments could be made as to the patentability of the claim, such arguments are deemed to

be unnecessary in view of the amendments to the base claim.

Claim 5 has been amended to clarify that the identifier is a compression mask having one bit associated with each of the plurality of ordered fields. There is a single identifier for each *sequence* of control words. This is in contrast to Tanaka where there is a plurality of compression masks, one for every control word in a sequence of control words. The scope of the claim 5 is unchanged by this amendment.

Claims 6, 8 and 9. Claim 6 calls for fetching an identifier that identifies a set of aligned fields removed during compression of the sequence of multiple-instruction control words. This is not taught by Tanaka. As described above, the compressed representation 701 in figure 6 of Tanaka contains the same number of fields (4) as the uncompressed representation 700. Thus no field has been removed. In particular, no aligned fields have been removed, since instructions from fields a, b, c and d are still present in representation 701.

Claim 6 further calls for reconstructing a corresponding uncompressed control word by inserting NOP instructions into the compressed control word in accordance with the identifier. This is not taught by Tanaka. Referring to the representation 720 of Tanaka's Figure 6, the third decompressed instruction word is not obtained from the third compressed instruction word, since its instructions are in the second compressed instruction word. Further, in Tanaka the decompressed word is not obtained by merely inserting NOP's; the position of the fields is also altered.

Claim 8 includes the element of disabling unused elements of the processor in accordance with the identifier. In contrast, Tanaka the processing element 110b in figure 12 is controlled by signal 400c. Referring to figure 11, signal 400c is a cache hit signal. This signal depends on whether an instruction has been loaded from a main memory (5 in figure 5) into an instruction cache 100a. In Tanaka, the mask information 410 is reported through signal line 410, which controls the selectors 120 – not the processing unit 110.

Claim 9 depends from claim 6. Although additional arguments could be made as to the patentability of the claim, such arguments are deemed to be unnecessary in view of the amendments to the base claim.

Claims 10-12. The system of claim 10 includes a mask latch for storing a compression mask that identifies a set of aligned fields removed during compression of the sequence of multiple-instruction control words. Tanaka does not teach the use of a compression mask that identifies a set of aligned fields removed during compression of the sequence of multiple-instruction control words. Rather, Tanaka's mask identifies the fields where compressed instruction should be placed – no aligned fields have been removed.

Claim 10 further calls for a pipelined permute unit, coupled to the logic unit and the memory and operable to reconstruct multiple-instruction control words by fetching a compressed multiple-instruction control word from the memory and inserting NOP instructions in accordance with the compression mask. The examiner refers to Tanaka column 3, lines 6-13. However, in column 3, lines 14-33 Tanaka teaches away from the use of a pipeline for

parallel processing in VLIW processor. In column 6, lines 1-2 Tanaka talks about inserting a NOP into an instruction field but makes no mention of how this achieved. In particular, Tanaka does not teach or otherwise suggest the use of pipelined permute unit.

Claim 11 depends from claim 10. Although additional arguments could be made as to the patentability of the claim, such arguments are deemed to be unnecessary in view of the amendments to the base claim.

Claim 12 calls for the compression mask to be used to disable processing elements of the plurality of processing elements that are unused by the sequence of multiple-instruction control words. As discussed above with reference to claim 8, the compression mask of Tanaka does not indicate which aligned fields were removed during compression of a sequence of instruction words. Rather, it indicates where in the uncompressed word the field values should be placed. Thus the compression mask of Tanaka is not equivalent to the compression mask of claim 12.

In light of the foregoing amendment and remarks, Applicant respectfully submits that the Tanaka reference does not teach, suggest, disclose or otherwise anticipate the recitations of claims 1, 4-6 and 8-12. Applicant thus respectfully requests that this basis of rejection of the claims be withdrawn and that a Notice of Allowance for these claims be mailed at the Examiner's earliest convenience.

Rejection of claims under 35 USC §103

Claim 2. The Examiner acknowledges that the Tanaka reference fails to teach, disclose or suggest the recitation of claim 2, and relies upon the

teachings of Mehrotra (US 6,571,016) to overcome this defect. 2. Applicant respectfully traverses this rejection of the claims. Claim 2, which depends from claim 1, relates to a method for compressing multiple instruction control words of a computation loop, whereas Mehrotra is concerned with compressing and decompressing video information. It is likely that Mehrotra's program of instructions for performing compression of video images includes computation loops, however, Mehrotra provides no teaching that the instructions in these loops are themselves compressed. The instructions control a computer to perform video compression. As described above with reference to claim 1, the method of instruction compression of claim 2 may be performed manually or by a computer. Applicant submits that there is no *prima facie* case for combining a reference on instruction word compression with a reference on video signal compression. The examiner states that "the use of Mehrotra could provide Tanaka the ability to repeat the performance of a specific computation (i.e. the decompression) at subsequent processing cycle". However, claim 2 relates to compression, not decompression. The compression process may be performed in a very different manner to the decompression process (for example the compression may be performed manually or in a non-time critical manner by a compiler, while the decompression may be performed by a processor executing the sequence of instructions).

It can be seen in light of the foregoing discussion of Mehrotra reference, however, that even if one were to combine the Tanaka reference with Mehrotra, the result would not be the claimed invention of claim 2.

In light of the foregoing remarks, Applicant respectfully submits that the Tanaka and Mehrotra references, whether considered alone or in combination fail to teach, disclose, suggest or otherwise render obvious the recitations of claim 2. Applicant thus respectfully requests that this basis of rejection of the claim be withdrawn and that a Notice of Allowance for claim 2 be mailed at the Examiner's earliest convenience.

Claims 3 and 13. The Examiner acknowledges that the Tanaka reference fails to teach, disclose or suggest the recitation of claims 3 and 13, and relies upon the teachings of Pechanek (US 6,173,389) to overcome this defect. Applicant respectfully traverses this rejection of the claims.

Claim 3, which depends from claim 1, is a method for compressing a sequence of instruction words by removing an aligned field from all of the words in the sequence (i.e. the same field is removed from every instruction word in the sequence). This process shortens the instruction words, but does not reduce the number of instructions words. In contrast, both Tanaka and Pechanek treat each field value as a short instruction word (SIW) and store the short instruction words together with information to allow the VLIW. Tanaka (See Figure 6) packs four SIW into the same space as a VLIW, but the field order is not maintained. Pechanek just stores the SIW. All of the approaches reduce the amount of memory required to store the instructions, however, Pechanek and Tanaka both require information on how to rebuild each VLIW, whereas in claim 3 each VLIW is decompressed in the same way (since each VLIW was compressed by removing the same field or fields). See Pechanek column 3, lines 2-4, for example. The approaches of Tanaka and

Pechanek achieve high compression ratios, but they require relatively complex circuitry to rearrange the VLIW slices (the SIWs). Rearrangement of the VLIW is not required for the method of claim 3, since the fields remain aligned in the compressed instructions.

Claim 13 depends from claims 10 and 12. As discussed above with respect to claim 3, both Tanaka and Pechanek require relatively complex circuitry to rearrange the slices of the VLIW from the compressed instructions. This is because the positions of the slices of the VLIW are not maintained in the compressed representation. In contrast, in claim 13 only NOPs in *aligned* fields (slices) are removed during compression, so the remaining slices are still aligned and no rearrangement is necessary. This results in less complex decompression circuitry. A single compression mask may be used for each loop. In a vector processor loops are often repeated many times. Having a single compression mask means that the hardware need be configured only once for the loop (for example, a processing element or memory bank may be disabled for the whole execution of the loop). In contrast, Tanaka requires a compression mask for each instruction of the loop. Pechanek does not cure this defect, since each VLIW is built up from SIWs. For example, Pechanek figure 5 teaches that each VLIW 510 includes enable mask bits (bits 10-17).

It can be seen in light of the foregoing discussion of Pechanek reference, however, that even if one were to combine the Tanaka reference with Pechanek, the result would not be the claimed invention of claims 3 and 13.

In light of the foregoing remarks, Applicant respectfully submits that the Tanaka and Pechanek references, whether considered alone or in

combination fail to teach, disclose, suggest or otherwise render obvious the recitations of claims 3 and 13. Applicant thus respectfully requests that this basis of rejection of the claim be withdrawn and that a Notice of Allowance for claims 3 and 13 be mailed at the Examiner's earliest convenience.

Claim 7. The Examiner acknowledges that the Tanaka reference fails to teach, disclose or suggest the recitation of claim 7, and relies upon the teachings of Shebanow (US 5,367,494) to overcome this defect. Applicant respectfully traverses this rejection of the claims. Claim 7, which depends from claim 6, calls for storing each control word compressed sequence of control words in the enabled subset of memory banks. Referring to Tanaka figure 6, even if the main memory 710 or the cache memory 720 were banked memory (and this is not taught or otherwise suggested by Tanaka), it would have four banks, a, b, c and d. All four banks must be enabled because the number of fields (slices) in the compressed control words 701 is the same as the number of slices in the uncompressed or decompressed control words. Even if the capability to disable memory banks were available (as taught by Shebanow), Tanaka cannot take advantage of this capability since all slices of the VLIW are in use.

In contrast, in claim 7 the control words are compressed by removing *aligned* fields. Each aligned field can be stored in a different memory bank. If an aligned field is removed, the corresponding memory bank may be disabled. Further, claim 7 calls for each compressed word in the sequence to be stored in the subset of enabled memory banks.

Still further, the cache memory 720 of Tanaka is used for storing *de*compressed instruction words. Applicant submits that the memory caches

of Tanaka are not equivalent to the memory banks of claim 7, since the memory banks of claim 7 store compressed words, whereas the cache memories of Tanaka store *de*compressed words. Thus, even if the combination of Tanaka and Shebanow suggested disabling a cache memory, the result would not the invention of claim 7.

In light of the foregoing remarks, Applicant respectfully submits that the Tanaka and Shebanow references, whether considered alone or in combination fail to teach, disclose, suggest or otherwise render obvious the recitations of claim 7. Applicant thus respectfully requests that this basis of rejection of the claim be withdrawn and that a Notice of Allowance for claim 7 be mailed at the Examiner's earliest convenience.

In light of the foregoing amendments and remarks, applicant submits that all rejections of claims 1-13 have been overcome. The scope of the amended claims is substantially the same with implicit meaning now made explicit. Allowance of claims 1-13 is therefore respectfully requested at the Examiner's earliest convenience. Although additional arguments could be made for the patentability of each of the claims, such arguments are believed unnecessary in view of the above discussion. The undersigned wishes to make it clear that not making such arguments at this time should not be construed as a concession or admission to any statement in the Office Action.

Please contact the undersigned if you have any questions regarding this application.

Respectfully submitted,

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